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PATENT APPLICATION

RESPONSE UNDER 37 CFR §1.116
EXPEDITED PROCEDURE
TECHNOLOGY CENTER ART UNIT 2822

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Nobuaki HASHIMOTO

Application No.: 09/856,627

Filed: May 24, 2001

Group Art Unit: 2822

Examiner: I. Soward

Docket No.: 109609

For: INTERCONNECT SUBSTRATE, SEMICONDUCTOR DEVICE, METHOD OF FABRICATING, INSPECTING AND MOUNTING THE SEMICONDUCTOR DEVICE, CIRCUIT BOARD, AND ELECTRONIC INSTRUMENT

AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR §1.116

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

In reply to the Office Action mailed November 19, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Please replace claims 1-4, 7, 10, 13, 19 and 20 as follows:

1. (Twice Amended) An interconnect substrate over which an interconnect pattern is formed, comprising:

a first portion; and

a second portion to be superposed on the first portion,

wherein the first portion has end parts as positioning references; and

wherein the second portion has a shape so as to be superposed on and inside the first portion except the end parts, the second portion positioned between the end parts.